Course Description

Course name	**Course 880 Wafer Fab Process Technology**
Duration	**4 days**
Format	**Public classroom or Inhouse event. Not suitable Online**

Overview

This intensive 4-day course, instructed by Mr. Jim Fraser, provides a broad overview of silicon wafer fab processing, with in-depth consideration of each of the many wafer fab process techniques – and associated materials and equipment – used to manufacture today's broad range of Si-based microchips.

Technical Focus

The computing power packed into a tiny microchip has exploded over the past several decades. A huge driver has been phenomenally successful in continuous evolution in microchip fabrication equipment, materials and techniques. With each new generation of chips, as devices are scaled ever tinier and performance requirements are ever more demanding, comes a wide range of exciting yet onerous new processing challenges, met head-on by highly motivated scientists and engineers. The course is not geared to a particular technology node; it considers the wide range of fab processes and technology nodes in volume production today.

Course Content

This 4-day course examines the entire wafer fab process, from Fab In through Parametric Test. (It also includes the details of raw Si wafer production.) Each processing technique is studied in turn. A baseline CMOS process flow is studied to introduce critical concepts of process integration. While knowledge of wafer fabrication would certainly be an asset, it is not a prerequisite. Participants will be encouraged to ask questions and participate in brief discussions. The highly detailed course notes provided will minimize the need for notetaking during class and will serve as an excellent useful post-course reference.

Who should attend?

This course is geared to a broad audience. While certainly technical in nature, it aims to also be highly practical, with a minimum of complex math and physics. Past participants have included scientists, engineers and technologists from a wide range of wafer fab equipment and materials supplier companies. Participants from wafer fabs include process engineers, equipment engineers, yield engineers, process integration engineers, product engineers, and technical managers.

Course daily schedule

Daily Schedule

Continuing Education Institute Professional Learning

The course material is arranged into 20 modules, five per day:

Module 1: Basics and Fundamentals; Semiconductor Devices and ICs
Initialisms and Acronyms
The Language of Wafer Fab
Brief History (e.g., evolution of electronic devices and ICs; scaling)
Electrical Conductivity
Semiconductor Devices (diodes, resistors, capacitors, transistors, MOSFETs)
Common CMOS Device Problems
Classification of ICs and IC Processes
Integrated Circuit Types
The Global Semiconductor Market

Module 2: Si Crystallinity, Crystal Defects, Crystal Growth
Crystallinity
Crystal Defects
From Sand to Silicon Wafer
Controlling Crystal Defects

Module 3: Baseline CMOS Process Flow
Summary of Wafer Fab Process Techniques
Baseline CMOS Process Flow (step by step)
Process Evolution

Module 4: Doping and Ion Implantation
Doping Fundamentals
Ion Implantation Fundamentals
Dopant Profiles
Crystal Damage & Annealing
Implant Equipment
Process Challenges
Process Monitoring & Characterization
Newer Doping Techniques

Module 5: Thermal Processing
Overview of Thermal Processing
Process Applications of SiO2
Thermal Oxidation
Thermal Diffusion
Thermal Annealing
Thermal Nitridation
Process Control
Thermal Processing Equipment
Newer Process Techniques (e.g., LSA, SPE, PO)

Module 6: Contamination Monitoring and Control
Forms and Effects

Sources and Control
Characterization and Measurement

Module 7: Wafer Cleaning and Surface Preparation
Wafer Cleaning Strategies
Chemical Cleaning
Aqueous Chemical Cleaning Equipment
Mechanical Cleaning
Newer Techniques (e.g., SCCO2, MD)

Module 8: Thin Films
Definitions
Film Formation Techniques
Important Properties
Metrology

Module 9: Vacuum Fundamentals, Plasma Fundamentals
Gas-Solid/Liquid Interactions
Vacuum Pumps
Wafer Fab Vacuum Systems
Plasma Basics
DC Diode Glow-Discharge Plasma Source
RF and HD Plasma Sources

Module 10: CVD 1: Basics, LPCVD, Epitaxy
CVD Basics
LPCVD Films
LPCVD Nitride/Poly Deposition Equipment
Epi Basics
Epi Process Applications
Epi Deposition Process
Epi Deposition Equipment

Module 11: PVD
PVD (Physical Vapour Deposition) Basics
Sputter Deposition Process
PVD Equipment
Step Coverage and Contact/Via Hole Filling
Metal Film Evaluation
Electrostatic Chucks

Module 12: Lithography 1: Photoresist Processing
Basic Lithography Process
Photoresist Materials
DUV Photoresist Process Flow
Photoresist Processing Systems

Module 13: Lithography 2: Image Formation
Basic Optics
Imaging
Overview of Imaging Equipment
Actinic Illumination
Exposure Tools

Module 14: Lithography 3: Registration, Reticles, RETs
Registration
Reticles
Resolution Enhancement Techniques (RETs)
The Evolution of Optical Lithography (EUV)

Module 15: Etch
Etch Terminology
Wet Etch Chemistries and Equipment
Dry Etch Processes
Physics and Chemistry of Plasma Etching
Dry Etch Applications
Dry Etch Equipment

Module 16: CVD 2: PECVD
CVD Basics
PECVD Equipment
CVD Films
Step Coverage

Module 17: CMP
Planarization Basics
CMP Basics
CMP Processes
Process Challenges
Equipment
Process Control

Module 18: Process Evolution 1 (Bulk Metals, IMDs); Cu ECD
Process Evolution
Al-based Interconnect
The Need for Cu and low-k IMDs
Damascene Process
Cu ECD
Low-κ IMDs
Cu Integration Challenges
Next Generation Metals

Module 19: Process Evolution 2: Gate Dielectrics, Silicides, Gates
Process Evolution
Evolution of Gate & Capacitor Dielectrics
Evolution of Silicides
Evolution of Transistor Gates

Module 20: ALD, finFETs, Misc. Processing Techniques
Atomic Layer Deposition (ALD)
Silicon on Insulator (SOI) Technology
Strained Silicon
FinFETs and Other Non-traditional Transistor Designs
3-D NAND Flash Memory
Wafer Fab's Environmental Footprint

Instructor biography

Mr. Jim Frazer

Founder of JFTS, Ottawa, Canada. Mr. Fraser has been a member of the Continuing Education Institute-Europe faculty since 2024.

Jim Fraser received his B.Sc. degree in Physics from McGill University in Montreal, Quebec, Canada. He has 23 years of intimate, hands-on experience in silicon wafer fab process engineering and engineering management at Nortel Networks and STMicroelectronics.
Jim has provided process analysis and documentation services pertaining to reverse engineering of a range of state-of-the-art microprocessors and related microchips at Chipworks (now TechInsights). He has also provided semiconductor patent research support for Chipworks.
Jim's technical training repertoire includes the courses "Silicon Wafer Fabrication" at Algonquin College and "Microelectronic Manufacturing Processes" at the University of Ottawa (both in Ottawa, Canada). More recently, he has delivered a range of silicon wafer fab process technology training courses on contract to the semiconductor industry, in North America, Europe and Asia.
Mr. Fraser has been a member of the Continuing Education Institute-Europe Faculty since 2024.